L. F. Miller

Controlled Collapse Reflow Chip Joining*

Abstract: Solder reflow connection of semiconductor devices to substrates has been shown to be a reliable, effective, and readily automated technique. Rigid copper spheres, which remain rigid during solder reflow, have been used successfully for some time as a major element of the contact joint. However, to expand the capability of such joints to larger devices such as multiple-transistor chips in hybrid components, ductile metallic joining pads can be used on the devices instead of the copper spheres to reduce mechanical strains and permit multi-pad devices to make proper contact to module lands during reflow. This paper describes a technique that prevents these solder pads from collapsing and permits large scale production. Termed "controlled collapse," the method is based on limiting the solderable area of the substrate lands and chip contact terminals so that surface tension in the molten pad and land solder supports the device until the joint solidifies. The result is a sturdy, testable connection of high reliability (bond strength 30-50 gm, pilot-production yields exceeding 97%, predicted failure rate—based on laboratory tests—considerably lower than that of copper ball contacts). The process is economically adaptable to automation and offers considerable latitude in fabrication and control tolerances.

Introduction

The component industry has developed a number of processes for joining semiconductor devices face down to carrier modules,[1-3] but these can generally be classified within two principal categories—dry and wet process. The dry processes can be represented by essentially solid state metallurgical interactions, such as thermocompression or ultrasonic bonding.[4,5] Wet processes generally take the form of solder reflow, such as in IBM's SLT module fabrication.[6] This paper is concerned with a particular wet solder reflow process, called "controlled collapse" and employing ductile metallic pads which are heat-reflowed to form the connecting joints. Significant economic advantages are attainable, as has been demonstrated through recent use of the process with the same automated equipment used for processing SLT modules.

Face-down ("flipped") semiconductor devices have often used rigid contacts (such as copper balls) to ensure support during joining, because diced devices might be electrically shorted if their contacts were to collapse when heated and allow the device edges to contact any conductive material.[7] However, if collapse-induced shorting is prevented, soft solder pads provide significant advantages since their ductility permits them to tolerate considerable stress during thermal cycling and leads to reduced strain and fewer contact failures. Furthermore, since solders are both malleable and capable of distortion (particularly when molten—as during chip joining), some lack of planarity in the pads or lands to which they are joined can be tolerated in the chip joining process. Thus multi-pad devices of significant size and complexity can be handled when the problem of edge shorting is eliminated.

The processes discussed here not only prevent reflowed solder pad devices from completely collapsing but, in fact, achieve a significant height of standoff for greater pad reliability. The techniques are based on limiting the solderable areas of both the device and substrate so that surface tension in the molten joint solder elevates the device. The use of surface tension in this way reduces the need for complex joining equipment and can permit wider control tolerances than other known methods.

The first section of this paper describes and compares several variations of the controlled collapse process; the second section provides a summary discussion of the module materials involved.

Process

Before discussing the process, it might be helpful to describe the components being considered. The silicon devices, or chips (Fig. 1), have electrical contact pad areas which are metallized with solderable materials (e.g., a layer of chromium to bond to the glass, a layer of copper for solderability, and a very thin layer of gold to protect the copper from oxidizing[7]). The solder itself is then deposited on these metallized pads.[8] In this work, lead-tin alloys with high lead concentrations were used primarily,

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* The process described herein was also described at the Hybrid Microelectronics Symposium, Society for Hybrid Microelectronics, Chicago, Ill., Oct. 28–30, 1968; the materials were described at the National Electronic Packaging and Production Conference (NEPCON), Anaheim, California, Feb. 13, 1969.

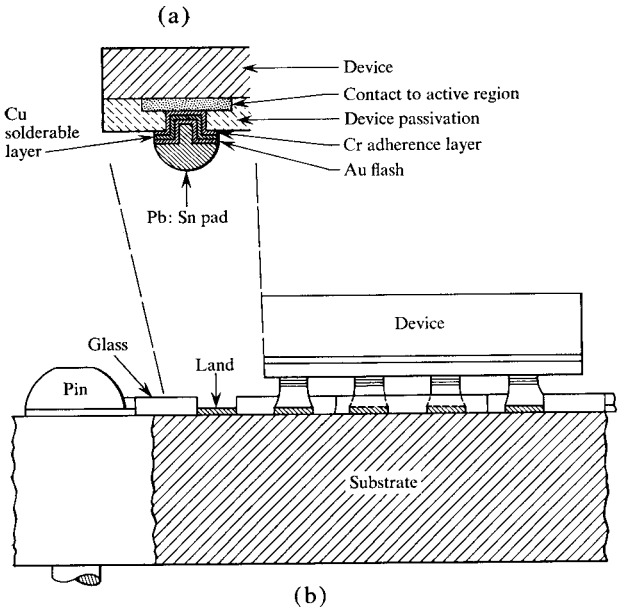
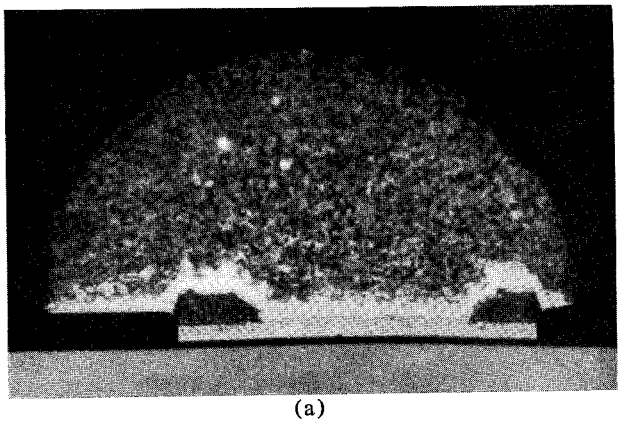


Figure 1 (a) Side view of a device; (b) side view of a device on a substrate (dam method).

Figure 2 (a) Cross-section of "wetback" solder pad; (b) device joined to ceramic with solder pad. (Photographs by M. Ricker.)



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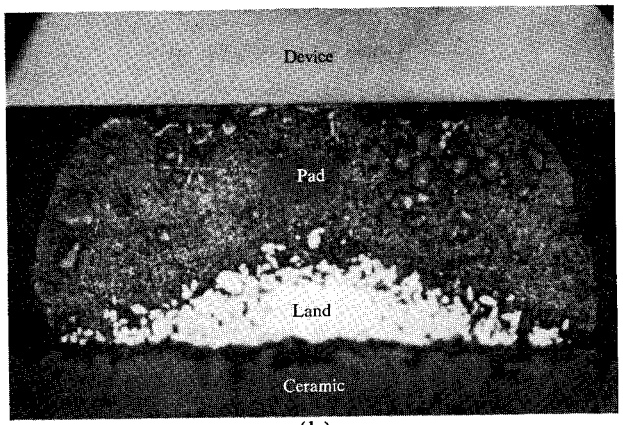

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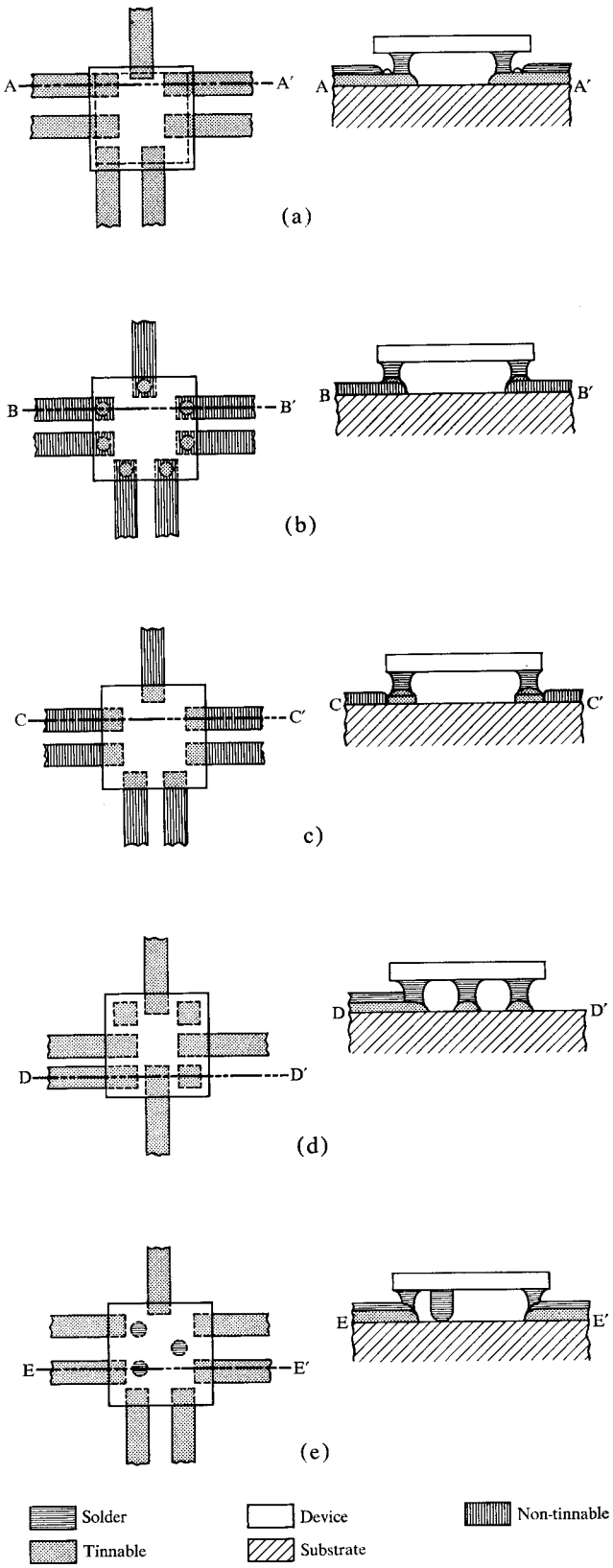


Figure 3 Illustration of the methods compared in Table 1. (a) Dams; (b) dots; (c) overlap; (d) extra pads on module; (e) extra pads on device.

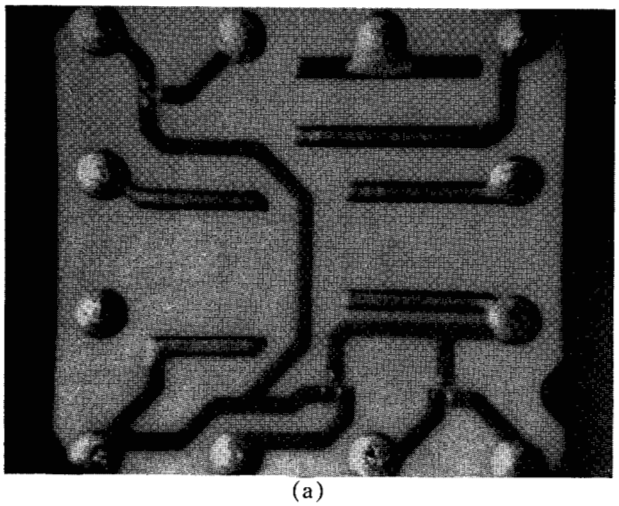
Table 1. Comparison of methods.

Method	*Procedure*	*Advantages*	*Disadvantages*
Dams	1. Screen, dry, fire tinnable conductive lands. 2. Screen, dry, fire or cure solder stop-off dams across finger ends. 3. Pin and tin module. 4. Join devices. (Example: glass dams on Ag: Pd lands)	1. No shorting of adjacent lands. 2. Same dam material can be used for crossovers (if glass), or overcoating (if polymer). 3. No new metallurgical compatibility usually required.	1. Tinning tends to give some difficulty. 2. Resistance may be higher under dam.
Dots	1. Screen, dry, fire non-tinnable lands. 2. Screen tinnable dots and other tinnable areas (as pin areas), dry and fire. 3. Pin and tin modules. 4. Join devices. (Example: gold non-tinning lands, Ag bearing dot.)	1. Potentially better tinning 2. Slightly easier registration. 3. Minimal silver migration. 4. Potentially better conductance.	1. Adhesion of dot. 2. Possibility of dot bleeding out to cause electrical shorting. 3. Proper metallurgical systems are difficult to optimize. 4. If crossovers are required, this process does not help.
Overlap	1. Screen, dry, fire isolated tinnable regions. 2. Connect these with non-tinnable lines, fire. 3. Pin and tin modules 4. Join devices (Example: Pt or Ag: Pd tinnable regions connected by Au, Ag:Pd; or Au:Pt non-tinning lines.)	1. Less adhesion compatibility required than with dots. 2. Simpler to use inert finger ends (as Pt).	1. Difficult to screen well. 2. Registration is quite critical.
Extra pads on module	1. Screen, dry, fire all tinnable regions. 2. Pin and tin modules. 3. Join devices. (Example: any tinnable land.)	1. Only one screening 2. Better tinning yield.	1. Sacrifice of electrically useful space on silicon. 2. Requires balanced format. 3. Possible capacitive effects.
Extra pads on device	1. During device pad operation, deposit extra pads. 2. Prepare module in normal way. 3. Reflow devices. (Example: Pb:Sn pads)	1. Very low cost—no additional steps.	1. Requires space for extra pads on insulated portion of device. 2. Requires balanced format. 3. Possible capacitive effects. 4. Does not provide the self-alignment of other methods.

but other alloys are feasible and, in certain applications, may be necessary for metallurgical compatibility. The solder can be applied to the metallized pads by vacuum metallizing the lead-tin alloy in an oversized area around each pad and then heating it to form a hemispherical ball by reflow. Since the solder does not wet the oxide surfaces around the periphery of each pad during this first reflow operation, relatively large hemispheres can be formed. Typically, those used in this work were of the order of 4 or 5 mils in diameter (Fig. 2).

The substrates are generally pressed alumina ceramic tiles similar to those used in the SLT process, although considerable experimentation has been done on other ceramics and these can indeed be employed. The substrate metallization is generally produced with thick film screened lands, which will be discussed in some detail in the next section. The devices and modules (substrates) are made separately and joined to each other in reflow furnaces containing either inert or reducing atmospheres, such as nitrogen, argon, or forming gas.

The process involves restricting solderability to those spots on the module at which the chip pads will make contact, so that solder cannot run along the lands and cause the chip to collapse and thereby short in the land solder on the substrate. Many ways of accomplishing this are possible, but we will restrict most of the discussion to two typical process types, called "dots" and "dams" and to some variations of these (see Table 1 and Fig. 3).



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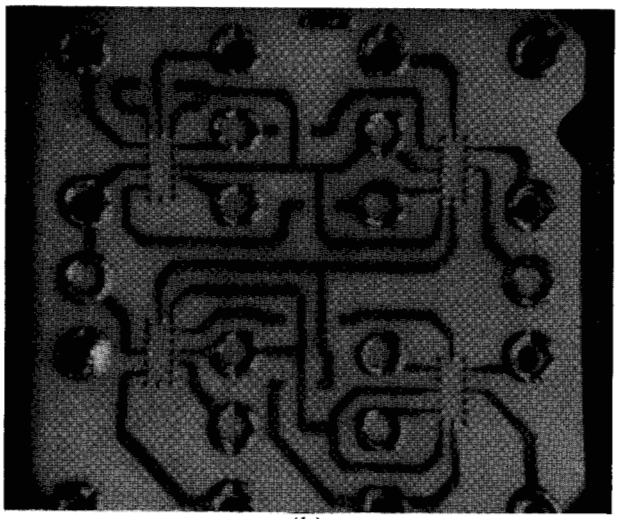


(b)

Figure 4 Two modules with combinations of tinnable and non-tinnable lands, and "dot" configurations at ends of lands. (Photograph, Fig. 4b, by L. Otten.)

• *Dots*

With this method, a circuit pattern is screened on the ceramic substrate with a non-tinnable electrode paste (discussed later) which is dried and fired. The tips of the fingers to which the device pads will be joined, as well as any areas which must also be tinned to ensure a reliable interconnection (such as the area around pins), are then screened with normal, tinnable electrode paste. The module is again fired to sinter the tinnable area and bond it to the underlying non-tinned land. Any screened passive components that are required for module fabrication are then added and fired. Normal pinning and dip tinning operations follow. During the dip tinning operation (which is generally done in 90% Pb, 10% Sn solder), the solder adheres only to the pin areas and to each finger tip, but not to the non-tinnable land sections (Fig. 4).

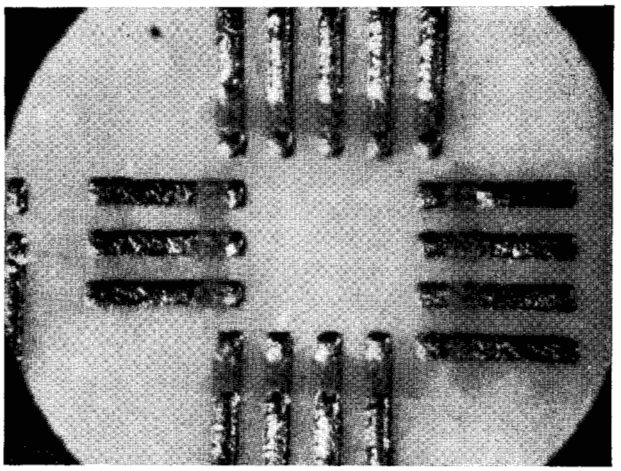


Figure 5 Dams (cured polyimide) on Ag:Pd lands — tinned. (Prepared and photographed by F. Glenn and K. Puttlitz.)

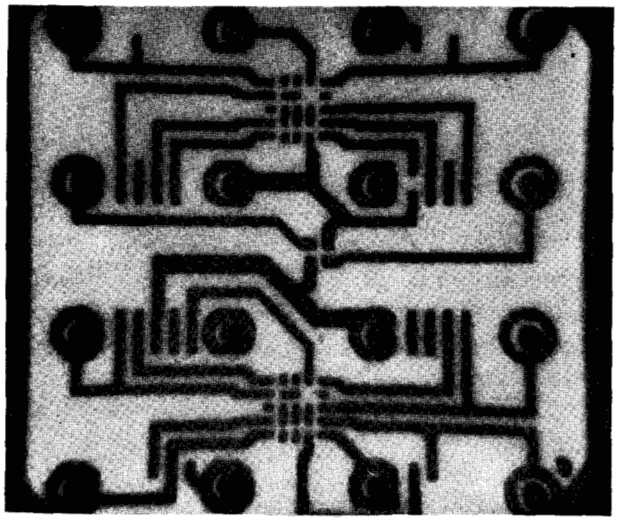
Devices with solder pads (and any other necessary components such as chip capacitors) are then reflow-bonded to the isolated tinned spots. Since the chip edges extend beyond the solder and since surface tension supports the device, collapse does not create shorting at the device edges.

• *Dams*

With this second method, the ends of normal screened and fired tinnable lands are delineated with a non-tinnable barrier. After firing or curing the barrier, or dam (which can be done simultaneously with the firing of other passive components, if desired), and after pinning, solder is deposited on non-covered land sections. As in the dot method, this allows isolated solder spots on the finger ends to receive the device solder pads (Fig. 5). The untinned area again prevents collapse-induced shorting since the chips remain suspended several mils above the lands; the untinned areas do not touch them. Many types of solder stopoffs can be used for this process and some of these will be discussed. This method has received particular emphasis at IBM.

• *Overlap*

This method may be considered the inverse of the dot process; instead of depositing the untinned lands first, the tinnable sections are deposited and fired and then interconnected with non-tinnable land patterns. A significant difficulty here is the maintenance of good land definition at the overlap region. Electrode paste can be squeezed under the screen or mask (which might be lifted by the previously printed and fired tinnable areas), and the dimensions can be difficult to control. Thus, although this method is certainly feasible, the others are considered somewhat easier to employ.



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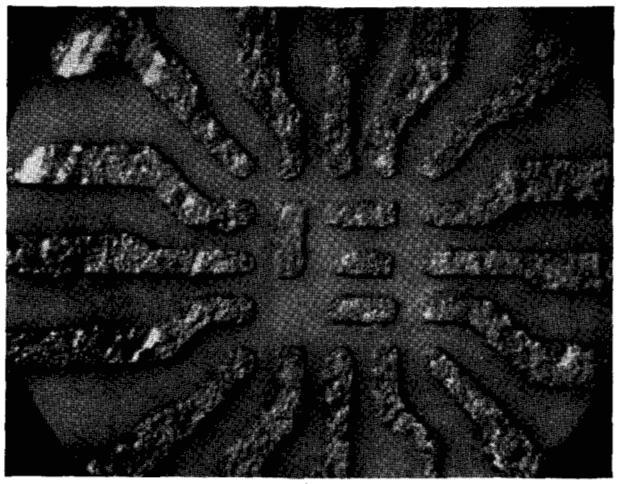

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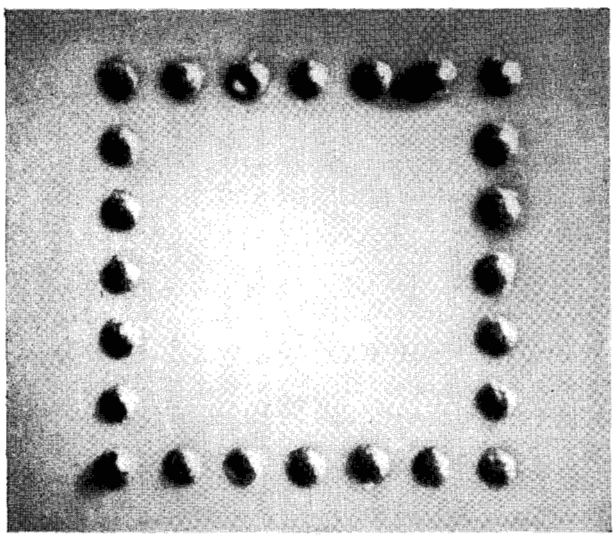

(c)

Figure 6 (a) Land pattern (dried) using extra pads which can prevent collapse; (b) extra pad configuration, etched from copper (screened resist); (c) isolated pads on ceramic.

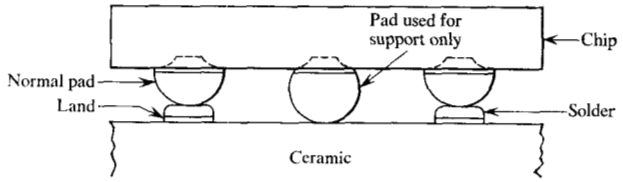

Figure 7 Side view of extra standoff pad on device, used to prevent collapse.

• *Isolated lands*

Not all of the lands must have this solder-wettable area defined; if just a few are so defined, perhaps three or four sites out of twenty or so on a device, the surface tension of those isolated pad areas is sufficient to maintain separation. The isolated areas on the modules do not have to provide electrical contact, but can serve merely as mechanical supports (Fig. 6). It has been calculated and demonstrated that the surface tension forces in the scheme described here can support considerably more weight—at least 30 times more—than they do.[9] There are possible disadvantages to this variation, however, including some sacrifice of electrically useful silicon area if more pads are used than are necessary to establish the electrical contact, possible capacitive effects from these extra pads, and possibly lower chip elevation than would exist if all pads were to serve as supports.

• *Extra pads*

Extra pads can also be placed on the chip, with no corresponding wettable land portion on the module (Fig. 7). Since the solder on the pads cannot wet the ceramic module surface, the surface tension of these extra pads will maintain the chip at an adequate distance from the substrate.[10] Again, however, capacitive effects must be considered.

Other techniques for using extra, non-electrical supports—either on the module or on the chip—require careful choice as to number and location, or tipping will occur. When supports are used, the potential problems in pad planarity become more important than with the other systems discussed previously.

• *Common characteristics*

These processes have the following similar characteristics:

(1) The first three involve two screening operations—one with a tinnable conductor and the other with a non-tinnable material. All are compatible with normal semiconductor, thick film module processing, with only some minor modifications required for format changes and slight variations in process detail.

(2) Registration and alignment of the tinnable and non-tinnable sections is relatively critical in order to achieve the controlled collapse of the device. When tinnable spots

of about 4-8 mils are used with device pads of about 4-5 mils in diameter, the chips are normally suspended between 2 and 3 mils above the lands, providing good stress relief through the long ductile members.

(3) The devices are, to a large extent, self-aligning on the limited solder areas, so that when contact is made between a part of each solder pad on the device and the land solder, the chip will float into position during the reflow process. Considerable misalignment in chip placement registration can be tolerated in some geometries due to this correcting mechanism.

(4) Irregularly shaped pads, and even crushed pads, on the chips can be used, since during the reflow process these pads re-form to hemispherical shape and can be joined as well as initially uniform pads. Thus defects due to prior electrical tests are eliminated, and the probes do not damage the pad joints, as is possible with rigid pads.

(5) Chip joining yields above 97% have been routinely demonstrated; chips can be replaced as required. Joint strengths are very good, typically 50 gm per pad in tensile strength, equaling reflowed joints made in other ways with hard device pads. High reliability has been demonstrated, even with large devices.[11]

(6) The solders found to be particularly successful have been 95% Pb, 5% Sn for the device pads, joined to 90-10 solder on the lands. The devices are held down with soldering flux during the reflow, which can be done at about 340°C for this metallurgical system. More rapid reflow at temperatures close to the solder liquidus will minimize metallurgical problems.

(7) The methods are applicable to multiple devices on a single surface and to devices with many pads. Using screening technologies, module lines and spaces of 4 mils can be manufactured; some modifications in technology might be required to reduce line dimensions and separation beyond that for production purposes.

Although this particular discussion is directed toward thick film technology, these concepts can also be extended to thin film technology and even to normal copper-clad printed circuits, if the thermal expansion differences of the materials are not limiting. (See Fig. 6b as an illustration of etched lands.)

• *Discussion of process*

These methods have been shown to permit wide flexibility in module construction. Devices with pads approximately 5 mils in diameter have been joined equally well in configurations ranging from 3-pad SLT fingers (which are approximately 15 mils wide) to devices with many pads on centers as close as 8 mils. For manufacturers who produce modules using SLT-like processing, the impact on production equipment would be minimal, since the compatibility is obvious.[12]

The joining of any two bodies with dissimilar thermal expansion characteristics can potentially cause a reliability problem.[13] As devices become larger and larger, the difference in thermal expansion between the device silicon and the alumina of the ceramic tends to become increasingly important. However, due in part to the ductility of the solder pad joint, devices of the order of 60 to 80 mils square have been shown to be highly reliable after many hundreds of cycles through wide temperature excursions, such as from −40° to +150°C[11]; the upper limit of size has not been established. Theoretically, the farther the device is suspended from the ceramic—that is, the longer the ductile beam—the smaller the stress that will be transmitted during such thermal stress periods to the critical joints where the pads meet the device. These elongations can be achieved by the proper choice of volume of pad material and size of the tinnable areas, permitting the use of large devices.

The tensile strength exhibited routinely by these joints has been of the order of 30 to more than 50 grams per joint; such strength is well beyond that required by normal device joints. Typically, for example, thermocompression wire bonds average only approximately 2 to 7 grams per one-mil wire when the wires are pulled off.[4]

The reliability of "flip chip" devices has been shown to be excellent, as represented by billions of hours of field usage, coupled with correlation to laboratory stress tests.[14] SLT devices which use rigid copper balls as pads were reported to show a ball failure rate of about 0.00004% per thousand hours at a 90% confidence level. This enormous amount of field data is not yet available for the all-solder joints discussed here, but laboratory stress tests lead us to believe that a considerable improvement in joint reliability can be expected from the ductile joints.[11]

Pilot quantities of tens of thousands of modules using devices with more than 10 pads each have shown chip joining yields above 97% with the dam method. One hundred percent visual inspection of 500,000-600,000 joints showed no cold joints. These yields are equal or superior to any known joining scheme that has been developed to the point of pilot production. The very nature of the controlled collapse mechanism permits somewhat more flexibility in temperature, time, placement, and even dimensions than do other chip joining methods. This wider latitude in processing is one of the reasons yields are very high.

If modules containing active devices are cooled by direct immersion in liquid coolant,[15] better thermal dissipation can be achieved with flip-chip devices such as

these than with back-mounted devices; the liquid can circulate around all of the sides of a flip-chip device. The heat dissipation is particularly effective if thin metal heat sinks are fastened to the backs of the devices, expanding the area of the thermal path (Fig. 8). Thus the advantages of economy, reliability, ease of replacement, and yield for these processes can be extended to high power devices.

Another consideration is the replacement of devices on multi-chip modules. This has often been demonstrated, and devices joined even after the third or fourth replacement have shown strength equivalent to that of the initial devices. These "controlled collapse" chips do not necessarily require localized heating to replace adjacent chips—the entire module can be reheated.

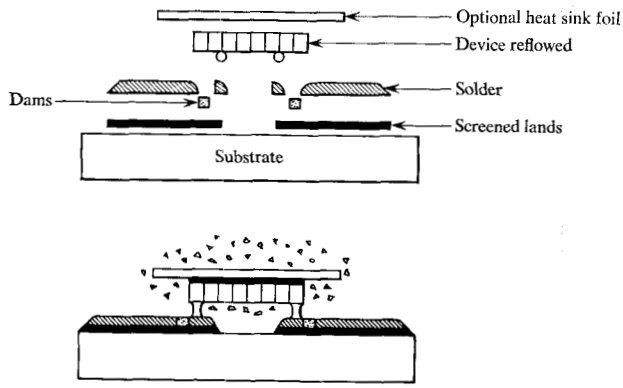

Figure 8 Flip chip with heat sink in boiling immersion-cooling liquid.

Materials

The materials described in this section have been used to demonstrate controlled collapse processes using existing SLT module fabricating equipment.[12] Thus, the development work was directed primarily toward screening operations which, within some limitation of line widths, conductivity, and circuit card compatibilities, demonstrated unique advantages of economy, flexibility, and reliability. This section will discuss the general types of screening materials and some considerations relating to their formulation, limitations, and performance. The following types of materials will be discussed: (1) tinnable lands; (2) non-tinnable lands; (3) solder stop-offs (dams); and (4) dots. The experimental data and conclusions described here were obtained under the same conditions as in references 16 and 17, where further detail can be found.

• *Tinnable lands*

Tinnable lands are used both to interconnect non-tinnable sections and to create tinnable dots. Since the latter may create special problems with respect to compatibility, they will be discussed later. The characteristics required of tinnable land materials for ductile pad processing are similar to those desirable in normal thick film processing: good adhesion, high conductivity, excellent screenability, low cost, high tinning yield, etc. Since a complete discussion of the technologies of these pastes would be prohibitively long here, only a few pertinent comments will be made, supplemented by Table 2,[17] which summarizes the properties of several pastes.

In the dam method, the solder layer is interrupted on the lands by the dams, and a high resistance section can result if the resistance of the untinned land is high. For circuits

Table 2. Summary of paste properties.

Property	*Type of paste* Ag : Pd	Au : Pt	Ag : Au : Pd	Au : Pt : Pd
Land density	G	problem	porous	G
Adhesion-tensile (psi)	2300–4000	2500–4000	2000–3000	3900–5000
Wetting by solder	G	G	G	G
Erosion by solder	F	F-G	F-G	G
Resistance (Ω/inch for a 200 mesh, 0.01-inch line)	1.5	6.5–10	5	7–10
Interaction with glaze	G	G	G	G
Reproducibility	G	F	F–G	G
Density (gm/cm³)	3.1	4.7	—	3.9
Cost/oz. (approx.)	$10	$60	$35	$60
Sensitivity to processing	G	P	F	G
Migration	F	G	G	G
Doped resistor compatibility	G	P	G	F
General reliability	G	G	G	G

G-good; F-fair; P-poor.

Table 3. Resistance and land height measurement for different screening conditions.

Metal	*Screen*	*Firing temperature in °C*	*Untinned resistance in ohms per inch, for land width of:*			*Land height in microns, for land width of:*		
			3 mils	*4 mils*	*5 mils*	*3 mils*	*4 mils*	*5 mils*
Ag : Pd	325 mesh	750	29.5–38	13.5–16	6.4–8.5	6–8	7–10	10–13
Ag : Pd	3-mil open mask	750	4.6–7.0	2.0–4.0	1.3–1.5	12–14	21–23	24–26
Ag : Pd	4-mil open mask	750	6.5–7.0	1.8–2.2	1.1–1.2			
Cu	Mesh mask	air 750 then forming gas 1000	3.2–6.5	2.8–6.5	1.0–4.0			
Cu	3-mil open mask		0.50–0.60	0.30–0.45	0.28–0.35	7–12	15–17	18–20
Cu	5-mil open mask				0.34–0.5			
Au	3-mil open mask	750	3.0–5.5	2.2–2.5	1.9–2.1	17–23	22–28	25–30
Au	4-mil open mask	750	5.0–6.0	1.6–2.3	1.3–1.6	10.5–13	17–28	25–27
			5 mils	*10 mils*	*15 mils*	*5 mils*	*10 mils*	*15 mils*
Ag : Pd	200 mesh	750	5.3	1.4	0.8			
Ag : Pd	2-mil cavity mask	750	5.3	1.4	0.9	10–12	24–25	23–24
Ag : Pd	3-mil cavity mask	750	4.0	1.0	0.6	13	21–32	23–32
Au	200 mesh	750	1.6	0.4	0.23			
Au	2-mil cavity mask	750	1.5	0.43	0.24	9–11	14–23	24–29
Au	3-mil cavity mask	750	1.3	0.38	0.22	9–12	16–18	20–26

that cannot tolerate such areas of high resistance, it was found that an electrode formula containing a metals ratio of approximately 80 parts of silver to 20 parts of palladuim would be useful. Although there is extensive literature on the migration of pure silver lands, it was found that the alloying effect of the palladium drastically reduces migration and permits these electrodes to be used in module fabrication.[16] As an example of the importance of the land resistance, even under a small dam section (depending on the line width), a silver-palladium land will show either no resistance change at all under a dam approximately 5 mils wide, or an increase in resistance on a 5 mil wide land up to about 0.05 ohm. In this form, commerically available gold-platinum lands would add about 0.2 to 0.7 ohm for the untinned section.

Depending on screening conditions, all pastes can produce a relatively wide range of land resistances. Thus, if wider or thicker lands are used, gross conductance increases can be attained, as shown in Table 3. By intelligent use of screens or masks, such as by increasing emulsion or mask thickness, eliminating the mesh or maximizing the size of the mesh holes, and adjusting "squeegee" angles and pressure, etc., significant improvements can be produced.

Land resistance is partially controlled by the interaction of the solder and the land, and also by the amount of solder deposited by the tinning process. The solder height can be increased by faster withdrawal rates from the molten solder and by lower solder bath temperatures. Of course, in any tinning operation, some compromise may be required by balancing such defects as bridging, unwet areas, and intermetallic brittleness with the desired solder height. Since most tinnable materials—and particularly silver- or gold-bearing materials—dissolve somewhat in molten solder, the amount of land material present is extremely important. Thin layers will obviously lose a larger proportion of metal into the solder than thicker layers.

• *Non-tinnable lands*

Non-tinnable lands can be used to connect tinnable areas and to produce conductive solder stop-offs (Fig. 4). The pastes are formulated similarly to those for tinnable lands—containing mixtures of powdered metals, frit, and organic vehicles to make them screenable—except that small quantities of finely dispersed non-tinnable particles are included to prevent interaction of the lands with solder.[18] Lands of this type do not accept solder or erode in solder, and resistance changes after tinning are negligible. Since these lands are not tinnable, metals, alloys, and frits which could normally not be used for tinnable lands become practical. For instance, non-tinning gold lands with good adhesion have been formulated, although tinnable gold lands are not very successful since gold dissolves readily in lead-tin solders. Thus, non-tinnable lands can potentially be made even more conductive and adherent, and in the case of silver, less migration-susceptible than tinnable lands. For example, it is known that magnesium

can be used as an inhibitor of silver migration in screened lands.[19] Magnesium might normally interfere with the tinnability of such lands, but if the lands are designed specifically to be non-tinnable this is not a detriment. (Of course, such a system might require firing in an inert or reducing atmosphere to avoid oxidizing the migration inhibitor, which increases cost and complexity.)

Another method for making non-tinnable lands involves firing the normally tinnable land on a ceramic substrate with which it can interact during firing. When the glazed material from the ceramic surface enters the structure of the electrode, the lands become non-tinnable. The glasses contained in the ceramic surfaces which perform this interaction have a relatively low softening point.

The non-tinning agents are used in relatively small amounts, typically 1 to 4 percent by weight of the formulation. The actual amount depends primarily upon the type of non-tinning agent, the kind of frit in the paste, and the metals in the paste.

Type of agent

To make the non-tinning filler most effective, the finest dispersion possible is required. Laboratory studies show that the most predictive measurement is the oil absorption value of the powder. The amount of material needed to prevent tinning showed less correlation with particle size or surface area measurement. High oil absorption value (or small particle size) is desirable. Oxides with high decomposition temperatures (preferably over 1000°C) and high free energies of formation have been found suitable. Colloidal powders such as the oxides of silicon, aluminum, indium, chromium, etc. have also been used. For most applications, however, colloidal silica (such as Cabosil*) is particularly effective. In addition, organometallics, polymers, or salts which decompose during firing to form such oxides have also been used to advantage.

Electron microprobe analysis of non-tinning silver-palladium lands has shown that the colloidal particles are well dispersed throughout the fired land, and that they frequently interrupt the land surface. These apparently prevent the solder from wetting and spreading on the land. The surface tension of the solder probably prevents intimate contact of the solder with metallic regions between the silica "islands".

Interestingly, tinning can be restored to the lands by polishing (which apparently smears a layer of metal over the untinnable spots). Thus, some care should be taken to prevent abrasion of the fired lands before the tinning operation. It is also feasible to locally polish sections where tinning is desired and thus avoid an extra screening step. Such a procedure has been demonstrated and shown to work, but the tooling might be extensive compared with that required by some of these other methods.

* Trade name, G. Cabot Corp., Boston, Mass.

Frit

The frit, flux, or binder in the paste can either enhance or deter the action of the non-tinning agent. If the frit does not interact chemically with the non-tinning agent, it can help stop the tinning of the land, particularly if it is a glass that is not reducible and has a high melting temperature. However, some frits of lower melting temperature hinder the effect of colloidal silica, requiring more silica to be used than if no frit were present. This was observed with both silver-palladium and gold non-tinnable pastes when Drakenfeld E1313 glass (a lead aluminum borosilicate) was used with Cabosil. Larger amounts of appropriately fine particle frits, such as 10 percent of Kimble TM7 glass (a relatively non-reducible glass) in either silver-palladium or gold pastes, also stopped tinning without any additional agents. Another example (combining a frit and decomposable silicone vehicle to prevent tinning) was demonstrated with silver-palladium and a combination of barium fluoride and barium borate flux with a vehicle containing Dow Corning R-5071 silicone resin. Chemicals such as barium acetate (which decomposes to form high melting oxides), have also been shown to be effective.

Metals

For reasons not well understood, different land systems respond differently to this non-tinning treatment. Not only do different metals require different amounts of non-tinning agents, but some non-tinning agents are relatively ineffective with some metals. For example, Cabosil works well for gold, platinum, silver-palladium, and silver-platinum lands, but not for gold-platinum.

Characteristics of non-tinnable lands

Any dilution of metals in a paste can be expected to increase electrical resistance unless the paste transfer, metal sintering, or resulting land thicknesses are simultaneously increased. Depending on the volume relationships, the dilution of metals with non-tinning agents generally increases resistance. The densities of the noble metals used in conductors are commonly about 10 to 21 gm/cm^3, while non-tinning agents are in the range of about 2.5 to 5 gm/cm^3. Thus a 1 percent weight dilution with a non-tinning agent might contribute 5 to almost 10 percent of volume dilution. Table 4 compares some of the resistance values for typical tinning and non-tinning formulations. It can be seen that the dilution effects, although real, are not of great magnitude and are important only in critical formats.

Since adhesion tests on conductors are commonly performed on soldered lands, it is difficult to comparatively evaluate the adhesion of untinnable lands. Treatments to make the surface tinnable—such as polishing, plating, or firing on tinnable material, etc.—could possibly change the adhesion. For this reason, but with the exception to be

Table 4. Comparison of resistance values for workable tinning and non-tinning lands screened through 200 mesh.

Metal system	*Type of agent*	*Approximate resistance in ohms per inch at width of:*		
		5 mils	*10 mils*	*15 mils*
80 Ag: 20 Pd	Tinning	5–8	1.5–1.7	0.9–1.1
85 Ag: 15 Pd	N. T.	7.5–10	2.5–2.8	1.5–1.6
Gold	No agent, but erodes	2.0	0.6	0.35
Gold*	N. T.	1.5	0.4	0.25
Gold	N. T.	3.1–4.5	0.6–1.4	0.4–1.1
Ag	Tinning	0.6–0.9	0.17–0.25	0.13–0.17
Ag	N. T.		0.23	0.14

* 2-mil cavity, generally analogous to 200 mesh.

described later, no good adhesion values are available for these formulations. However, probing the lands with a scalpel (which can be correlated to strength testing) has indicated toughness and good adhesion for acceptable non-tinning formulations. The colloidal particles in non-tinning agents tend to increase paste viscosity, increase thixotropy, reduce flow, and increase the tendency to clog the screen during printing. This could be a significant problem since it is related to the need for a high solid content to achieve good conductance. Of course, rheological optimizations can be introduced with vehicle changes and proper surfactants to make these formulations usable, but generally they tend to produce pastes more difficult to screen than normal pastes. Fortunately, for many formulations the amount of non-tinning agent is relatively small, and one can therefore compensate for it.

• *Dams*

As previously mentioned, the non-tinning lands can be used as dams or solder interrupts when applied across regular tinnable lands. The principal reason for using a conductive dam is to prevent resistance increases in the dam area, but this is achieved only with properly compatible materials in the tinnable and non-tinnable formulae. Since alloying commonly increases resistance, dissimilar metals can be undesirable. For example, if the non-tinning land contains gold and the top lands contain silver, the dammed area may be of considerably higher resistance than if a non-alloying dam were used. On the other hand, if a non-tinning gold dam is placed across a tinnable gold-platinum land, the resistance of the dammed section is almost as low as if the area were soldered. The difficulty in using conductive dams is twofold: the matching of the metals is sometimes a problem, and there is some possibility of electrically shorting adjacent conductors when compaction of circuitry requires small spacings between them. Thus, for chips with closely spaced pads, it was found desirable to use glass or other nonconductive dams.

Many types of dams or stop-offs can be used and have been demonstrated, including glass, metal oxide, polymers, silica, and non-tinning conductors. Several basic attributes are important: the dams should interact as little as possible with the underlying conductive lands to avoid conductivity difficulties or tinnability problems at the finger ends; the dams should be of minimal thickness and width to reduce geometric shielding of the finger ends during tinning and to minimize the non-tinned area; and adhesion and stability should be assured throughout the life of the module. Furthermore, the material should be screenable, not excessively abrasive, and reproducible, and it should be able to protect the lands from corrosion (or at least not increase their corrosion susceptibility). Experiments with glass dams indicate that they should be fired at, or just above, the softening point to minimize bleeding into the tinnable land that interfaces with the solder (such as occurs with glazed substrates). Complete flowout and glazing of the glass is not necessary; the process requires just enough sintering of the particles to achieve solidity and firmness of the dam to prevent damage during further processing. If the glass pastes have low glass content, and if fine mesh screens or thin masks are used for printing, the desired sharply defined, low profile dams are obtained. Several types of glasses have been demonstrated, indicating that compatibility is achievable within a range of processing temperatures from about 550°C to more than 1000°C. The choices are numerous, and the matching of almost any set of module processing conditions is not considered difficult.

Metal oxides, which interact even less with lands than does glass, seem to permit better tinning of the finger ends. A particularly effective formulation contains palladium oxide fluxed with 3 percent of Corning 7720 glass. Dilute dispersions of colloidal silicas such as Cabosil also produce good solder stop-offs. However, if applied too thickly, cracking results when the modules are thermally cycled. This type of dam has the potential advantages of low cost, no abrasiveness (as with glass), and no interaction with the tinnability of the underlying lands.

High temperature polyimide resins have interesting advantages in that they can withstand soldering temperatures and thermal cycling, but do not have to be fired. Sharply defined, low profile dams have been fabricated with polyimides, without any deleterious land action. The polyimide area can also be extended, if desired, to provide overcoating protection. Both DuPont's PYRE ML varnish and PI4701 (with 10% Cabosil added to provide thixotropy) produced good dams with curing cycles under 300°C.

It would be an interesting extension to employ glazed resistors, which might normally be used on some electronic modules, to provide the dammed regions. However, because of the large amount of low-softening-point glass

in normal glazed resistor formulations, several attempts to use such pastes as dams failed due to the uncontrolled bleeding of the glass into the lands at the firing temperatures required to mature the resistors. This bleeding either completely prevented the tinning of finger ends or resulted in tinnable pad sections that were of irreproducible size. However, for non-critical regions, this might be a practical procedure.

• *Dots*

As previously described, dots of tinnable material on top of non-tinning lands can be used to define tinnable sections. With this method, compatibility of the two lands and the solder is the most important factor affecting adhesion, contact resistance, and tinnability. In some instances, it is relatively simple to obtain metallurgical compatibility; for example, untinnable silver-palladium lands with tinnable silver-palladium dots work very well. However, in this system the untinnable lands might be more susceptible to silver migration, since they do not have the protective solder layer found on tinnable silver-palladium lands. (Tests have shown that lead-tin solder on top of silver-palladium electrodes further retards migration.)

Better conductance can be achieved with non-tinning gold or copper lands than with silver-palladium. However, since the copper requires reducing or inert atmospheres for processing, the material and its environment need careful characterization before it can be used (as with such active metals as Mo, W, Ti, etc.), particularly with glass crossovers which might tend to be reduced. Such processing might also require extra equipment to deal with such atmospheres. Gold non-tinning lands are probably a good compromise, but compatibility with the tinnable dot and the solder presents problems. The adhesion to the underlying gold land of most tinnable dots that have been tried (such as platinum, gold-platinum, and ternary alloys of noble metals) is poor; the dots can be "flicked out" after they are fired. Silver-bearing dots, such as silver-palladium, adhere reasonably well, but the ratio of 80 parts silver to 20 parts palladium does not tin very well in lead-tin solder. This is apparently due to a change in the ratio when the silver is pulled out during firing to alloy with the gold in the underlying lands. However, a ratio of 85 parts silver to 15 parts palladium tins quite well, while higher silver ratios erode too readily in the solder. In general, unless the solder is already saturated with silver, silver from the lands will tend to dissolve quite rapidly during tinning. The most significant problem with this silver-palladium and non-tinning gold combination is that lead-tin solder weakens the joint and tends to dissolve the soluble silver-gold rich alloy around the dot periphery. However, this can be minimized if tin is eliminated from the solder, since it is mainly the tin which erodes both the dot and the underlying gold land. If there is silver in the solder, only the dot seems to be eroded, not the gold land.[20] Thus, the metallurgical compatibility of this system, as mentioned before, obviously involves the solder system.

A metallurgically compatible dot method offers the following advantages: high conductivity, minimal silver migration (silver does not readily form dendrites from a dot surrounded by silver-free conductive material since the electric fields are strongest at the conductor edges), excellent tinnability, and slightly less critical registration of the two screened portions. In elaboration of the last two advantages, (1) the tinnable dots are not in a "valley" as with dams, but instead are raised above the lands so that contact with the molten solder is excellent. On runs of several hundred parts tinning yields approaching 100 percent have been achieved with much less care required than with dams. (2) Since the dot shape is not dependent on registration, the land fingers can be extended beyond the normal chip pad positions so that minor malregistrations can be tolerated with some formats. The greatest limitation here is to avoid electrical shorting of the fingers with the conductive dam material if it seeps beyond the desired format during screening. Furthermore, for devices with relatively large pad spacings, the lands can be made quite large and the dots then have wide latitude for positioning within the land area.

Summary

With the processes and materials described above, face-down joining methods have been extended to higher density hybrid and monolithic applications. The result is a reliable, testable interconnection offering considerable flexibility in design and fabrication. Yields in pilot production have exceeded 97%, and automated manufacturing equipment has been shown to be adaptable to controlled collapse techniques.[21]

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